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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,797	01/13/2004	Wayne F. Ellis	BUR920030151US1	1796

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EXAMINER	
MERANT, GUERRIER	
ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,797	ELLIS ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial Office Action based on the application filed on January 13, 2004. Claims 7-26 are currently pending and have been considered below.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. As per claim 7: the phrases "means for allocating" is ambiguous because not clearly defined in the specification.

b. Claims 8-13 inherit the 35 U.S.C. 112, first and second paragraph issues of the independent claim 1 by virtue of their dependency.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7, 9-13, 14, 16-23 & 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Irrinki et al (US 5,987,632)** and further in view of **Kawagoe (US 6,243,307 B1).**

6. Claim 7: By using the phrases "means for", it appears the applicant is attempting to invoke U.S.C.112, 6th paragraph. However, the specification does not describe any specific structures (means) for performing these functions, thus U.S.C. 112 6th is not invoked.

7. As per claim 7: **Irrinki et al** substantially teaches an integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system, the architecture comprising:

c. a BIST *(e.g. item 120, fig. 1)* for identifying and transmitting row and column addresses from failed embedded memory *(e.g. col. 3, lines 56-63; col. 4, lines 6-17; col. 5, lines 20-52)*;

d. a first memory element *(e.g. items 310, 314, fig. 3)* for storing row addresses that have been assigned for repair by row redundancy *(e.g. col 6, lines 49-52)*;

e. a second memory element *(e.g. items 320, 324, fig. 3)* for storing repaired column addresses that have been assigned for repair or correction by column redundancy *(e.g. col. 6, lines 52-56).*

8. But **Irrinki et al** fails to explicitly teaches a third memory element for accumulating the failed row and column addresses transmitted from said BIST and assigning them a particular weight value based on the number of like addresses already accumulated in said third memory element and their relative locations within the

memory system; and means for allocating redundancy resources of the memory system. However, **Kawagoe** substantially teaches an integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system, the architecture comprising:

f. a BIST *(e.g. item 2010, fig. 2)* for identifying and transmitting row and column addresses from failed embedded memory *(e.g. col. 7, lines 34-44)*;

g. a first memory element *(e.g. item RM1, fig. 3)* for storing row addresses that have been assigned for repair by row redundancy *(e.g. col. 10, lines 60-64)*;

h. a second memory element *(e.g. item CM1, fig. 3)* for storing repaired column addresses that have been assigned for repair or correction by column redundancy *(e.g. col. 10, lines 65-67; col. 11, lines 1-2).*

i. a third memory element *(e.g. item 300, fig. 1)* for accumulating the failed row and column addresses transmitted from said BIST and assigning them a particular weight value based on the number of like addresses already accumulated in said third memory element and their relative locations *(column or row)* within the memory system; and means for allocating redundancy resources of the memory system *(e.g. 8, lines 65-67; col. 9, lines 1-17; Abstract).*

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement the circuit of **Irrinki et al** with the circuit of **Kawagoe** in order to provide a circuit capable of realize speedy detection of defective memory cell and redundancy analysis with a simple structure (e.g. col. 5, lines 28-35; **Kawagoe**).

9. As per claim 14: **Irrinki et al** substantially a method of providing BIST redundancy allocation to an embedded memory system, comprising the steps of:

j. a) identifying failed row and column addresses of defective memory blocks in said embedded memory system *(e.g. col. 3, lines 56-63; col. 4, lines 6-17; col. 5, lines 20-52)*;

d) and transferring said failed row and column addresses associated with the most fails from said third memory element to first *(e.g. items 310, 314, fig. 3)* and second memory elements *(e.g. items 320, 324, fig. 3)* according to a decision algorithm *(e.g. co.l 6, lines 49-56)*.

b) accumulating said failed row and column addresses identified in step a in a third memory element.

But **Irrinki et al** fails to explicitly teaches a third memory element for accumulating the failed row and column addresses transmitted from said BIST and assigning them a particular weight value based on the number of like addresses already accumulated in said third memory element and their relative locations within the memory system; and means for allocating redundancy resources of the memory system. However, **Kawagoe** substantially teaches a method for providing BIST redundancy allocation to an embedded memory system, the architecture comprising:

k. a BIST *(e.g. item 2010, fig. 2)* for identifying and transmitting row and column addresses from failed embedded memory *(e.g. col. 7, lines 34-44)*;

l. a first memory element *(e.g. item RM1, fig. 3)* for storing row addresses that have been assigned for repair by row redundancy *(e.g. col. 10, lines 60-64)*;

m. a second memory element *(e.g. item CM1, fig. 3)* for storing repaired column addresses that have been assigned for repair or correction by column redundancy *(e.g. col. 10, lines 65-67; col. 11, lines 1-2).*

n. a third memory element *(e.g. item 300, fig. 1)* for accumulating the failed row and column addresses transmitted from said BIST and assigning them a particular weight value based on the number of like addresses already accumulated in said third memory element and their relative locations *(column or row)* within the memory system; and means for allocating redundancy resources of the memory system *(e.g. 8, lines 65-67; col. 9, lines 1-17; Abstract).*

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement the method of **Irrinki et al** with the method of **Kawagoe** in order to provide a test method capable of realize speedy detection of defective memory cell and redundancy analysis with a simple structure (e.g. col. 5, lines 28-35; **Kawagoe**).

10. Claim 21: **Irrinki et al** substantially teaches an integrated circuit comprising:

o. an embedded memory system having a plurality of row and column redundancies (e.g. items 412 7 422, fig. 4)

p. a BIST *(e.g. item 120, fig. 1)* for identifying row and column addresses of defective memory blocks in said embedded memory system *(e.g. col. 3, lines 56-63; col. 4, lines 6-17; col. 5, lines 20-52)*;

q. a first memory element (e.g. item 314, fig. 3);

r. a second memory element (e.g. item 324, fig. 3).

But **Irrinki et al** fails to explicitly teaches a third memory element for accumulating the failed row and column addresses transmitted from said BIST and assigning them a particular weight value based on the number of like addresses already accumulated in said third memory element and their relative locations within the memory system; and means for allocating redundancy resources of the memory system. However, **Kawagoe** substantially teaches an integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system, the architecture comprising:

s. a BIST *(e.g. item 2010, fig. 2)* for identifying and transmitting row and column addresses from failed embedded memory *(e.g. col. 7, lines 34-44)*;

t. a first memory element *(e.g. item RM1, fig. 3)* for storing row addresses that have been assigned for repair by row redundancy *(e.g. col. 10, lines 60-64)*;

u. a second memory element *(e.g. item CM1, fig. 3)* for storing repaired column addresses that have been assigned for repair or correction by column redundancy *(e.g. col. 10, lines 65-67; col. 11, lines 1-2).*

v. a third memory element *(e.g. item 300, fig. 1)* for accumulating the failed row and column addresses transmitted from said BIST and assigning them a particular weight value based on the number of like addresses already

accumulated in said third memory element and their relative locations *(column or row)* within the memory system; and means for allocating redundancy resources of the memory system *(e.g. 8, lines 65-67; col. 9, lines 1-17; Abstract)*.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement the circuit of **Irrinki et al** with the circuit of **Kawagoe** in order to provide a circuit capable of realize speedy detection of defective memory cell and redundancy analysis with a simple structure (e.g. col. 5, lines 28-35; **Kawagoe**).

Claim 9: **Irrinki et al** and **Kawagoe** teach an integrated redundancy architecture as in claim 7 above, wherein said first memory element includes a register for storing row addresses that have been assigned for repair by row redundancy *(e.g. item 314, fig. 3;* **Irrinki et al** - row storage unit RM1, fig. 3; **Kawagoe)**.

Claim 10: **Irrinki et al** and **Kawagoe** teach an integrated redundancy architecture as in claim 7 above, wherein said second memory element includes a register for storing column addresses that have been assigned for repair by column redundancy *(e.g. item 324, fig. 3;* **Irrinki et al** – item *column address storage unit CM1, fig. 3;* **Kawagoe)**.

Claims 11 & 18: **Irrinki et al** and **Kawagoe** teach an integrated redundancy architecture/method as in claims 7 & 14 above, wherein said third memory element includes a register *(e.g. item 300, fig. 1)* for accumulating the failed row and column addresses transmitted from said BIST *(e.g. 8, lines 65-67; col. 9, lines 1-17; Abstract;* **Kawagoe***)*.

Claims 12-13, 19-20 & 22-23: **Irrinki et al** and **Kawagoe** teach an integrated redundancy architecture/method as in claims 7, 14 & 21 above, further comprising a finite state machine *(e.g. item 210, fig. 2;* **Irrinki et al**) having a decision algorithm, said finite state machine in electrical communication with said first memory element, said second memory element, and said third memory element *(e.g. col. 4, lines 55-67 & col. 5, lines 28-51;* **Irrinki et al**).

Claims 16 & 25: **Irrinki et al** and **Kawagoe** teach an integrated circuit and method as in claims 14 and 21 above, wherein said first memory element includes a register for storing said failed row addresses *(e.g. item 312, fig. 3;* **Irrinki et al**).

Claims 17 & 26: **Irrinki et al** and **Kawagoe** teach an integrated circuit and method as in claims 14 and 21 above, wherein said second memory element includes a register for storing said failed column addresses (e.g. item 322, fig. 3; **Irrinki et al**).

11. Claims 8, 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Irrinki et al** and **Kawagoe** as applied to claims 7, 14 and 21 above, and further in view of **Ohtani et al (US 2002/0196683 A1)**.

As per claims 8, 15 and 24: **Irrinki et al** and **Kawagoe** fail to teach said first, second, and third memory elements include the function of content addressable memory. However, **Ohtani et al** teaches a circuit/method for of providing BIST redundancy allocation to an embedded memory system comprising storage elements (e.g. items MCR11, MCR12, MCC11 fig. 3) and wherein the storage elements include the function of content addressable memory *(e.g. [0175], [0178], [0187]).*

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to replace the memory of **Irrinki et al** and **Kawagoe** with the memory of **Ohtani et al** in order to accomplish the same function.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

w. **Eustis et al (US 2005/0055173 A1)** teaches an integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system wherein a column is assigned a particular weight value based on the number of errors occurred (e.g. [0015]).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner
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8/11/07

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08/11/07